REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Lin et al.* (U.S. Patent No. 6,093,606). Claims 1-22 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Mandelman et al.* (U.S. Patent No. 6,541,815 B1). Applicants respectfully traverse these rejections.

Claims 23 – 112 are canceled without prejudice. Claims 1 and 21 have been amended to more clearly claim the subject matter that the Applicants' regard as the invention.

Lin et al. disclose a method for manufacturing vertically stacked gate flash memory devices. *Lin et al.* disclose at column 5, lines 9 – 18 and Figure1J that an ONO layer 30 is formed over the floating gate FG. Column 5, lines 49 – 57 and Figure 1L discuss and show that a control gate CG is formed over the ONO layer 30 such that the ONO layer 30 is formed between the floating gate FG and the control gate CG.

Applicants' invention is to a method for making an array of memory cells in which an ONO layer is formed over the substrate and a control gate is formed over the ONO layer. The nitride of the ONO layer is adapted to operate as the charge storage layer. This is not the same as *Line et al.* where the floating gate FG is separate from the ONO.

Additionally, Applicants' invention as claimed limits the memory cells to being spaced apart one half of a minimum pitch of the array. There is no such teaching in *Lin et al. Lin et al.*, therefore, neither teaches nor suggests Applicants' invention as claimed in the amended claims.

Mandelman et al. disclose a dual cell flash memory structure. Column 6, lines 63 – 66 teach that the first gate dielectric 28 can be an oxide, oxyntride, or a combination of these. Column 7, lines 16 – 22 states that a doped polysilicon layer 30 is formed over the first gate dielectric 28 to act as the floating gate region of the structure. Column 8, lines 20 – 49 describe forming the second gate dielectric 42 and the control gate 44. This neither teaches nor suggests Applicants' invention as claimed in the amended claims.

The present claims recite that a nitride layer is formed to operate as the charge storage layer. *Mandelman et al.* has a separate floating gate region 30 to act as the charge storage layer. Additionally, Mandelman et al. teaches that the memory cell structure is a $2F^2$ cell while the

present invention claims a multi-bit, F^2 cell structure. *Mandelman et al.*, therefore, neither teaches nor suggests Applicants' invention as claimed in the amended claims.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new subject matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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